REMARKS

Claims 1-29 were pending in this application and were each rejected. Claims 1-29 remain pending.

Reconsideration and full allowance of Claims 1-29 is respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to *Greenley et al.* ("Greenley") in view of U.S. Patent No. 5,706,481 to *Hannah, et al.* ("Hannah"). The Applicant respectfully traverses this rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443,*

PAGE 13/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

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1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

Claims 1, 14, and 23 recite a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claims 1 and 14 also recite a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claims 1 and 14 recite "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claims 1, 14, and 23 are crystal clear – the "shifter circuit" can process a data value before the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

The Examiner alleges that Greenley teaches

> A shifter circuit (Greenley 160,170 of Fig. 1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b) sign extending (Greenley Col. 2 lines 48-54), and c) zero extending (Greenley Col. 2 lines 45-47) said first data value prior to loading said first data value into said target register;

Greenley teaches, in col. 2, lines 19-54:

> Since needed data may not be physically stored consecutively in data cache 180, a LOAD access to data cache 180 must insure that the accessed data is aligned (i.e. both the upper and lower half of a word is fetched) into an appropriate format to write into a register in the register file 150. For example, when accessing a half-word from the data cache 180, the alignment unit 170 assures that the least significant bit of the half-word is in the least significant bit location in the register and the most significant bit of the half-word is in the bit position 15 in the register. After the word is aligned, it may be sign extended if the sign of the accessed word is ascertained during a signed load operation.
>
> Referring to FIG. 2, a detailed block diagram of the alignment unit 170 and the sign extension unit 160 coupled between the data cache 180 and a target register in the register file 150 is shown. The purpose of the alignment unit 170 is to right justify the data fetched from the data cache 180. For example, when a byte is fetched from the data cache 180, regardless of its byte position (i.e., 0 through 7) in the cache, the byte is always right justified in the alignment unit. Similarly, a half word is also right justified in the alignment unit 170, regardless of what position the half word occupied in the cache 180, or even if the two bytes of the half word were present in two different cache lines in the data cache 180. Words, double words, and extended words are

PAGE 15/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

> similarly aligned by the alignment unit 170. In an unsigned load operation, the rest of the register not loaded with actual data is zero filled.
>
> The purpose of the sign extension unit 160 is to fill in the unoccupied bits of a register with sign information indicative of the sign of the data loaded from the data cache 180. The sign of the data is determined by its most significant bit ("MSB"). For example, if the MSB of the data is a "0", the data is considered positive. On the other hand, if the MSB is a "1", then the data is considered negative.

The Examiner therefore claims that sign extension unit 160 and alignment unit 170 together form the claimed "shifter circuit." The Examiner is correct in that sign extension unit 160 does perform sign extending, and the alignment unit 170 does perform zero filling and shifting. In fact, Greenley teaches that the alignment must be assured, and that alignment unit 170 assures that the appropriate bits of the half-words are in the appropriate bit positions. *See col. 2, lines 19-30.* It is clear from this that, in Greenley's system, that the "shifter circuit" of 160/170 cannot be bypassed, as those functions must be present.

It is clear, then, that Greenley does not, and cannot, include "bypass circuitry" as claimed, and Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In Greenley, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, Greenley recites that all data passes through a shifter. More specifically, Greenley recites that all data passes through a shifter

PAGE 16/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

(the alignment unit 170 and the sign extension unit 160) before the data is stored in a register file 150.

The Examiner now references Hannah, and alleges that "Hannah has taught bypassing functions circuitry capable of transferring said first data value to said target without processing said first data value in said shifter circuit (Hannah column 9, lines 31-67; Figure 11; Figure 12, Figure 13, and Figure 14)." This passage actually teaches:

> FIG. 11 shows three examples of different configurations that can be used for the interpolator chains in the first configuration, four of the 4-bit untt 1101 can be stacked to perform 16-bit tri-linear interpolations. In the second configuration, a pair of the 8-bit unit 1102 can be stacked to perform the 16-bit tri-linear interpolations. In the third configuration, a single 12-bit unit 1103 is used to perform the interpolations. A number of multiplexers are programmed to couple the various units in order to achieve the desired configuration. In this manner, the same hardware can be utilized with minimal extra gate count to attain the flexibility in data width. In some applications, greater precision and resolution are desirable, Whereas, in other applications, speed and cost are of greater importance.
>
> In the currently preferred embodiment, the units 1101-1103 are comprised of an S-stage, a T-stage, and an LOD-stage. The S-stages are comprised of 4-bit slices 1104. The T-stages and LOD Stages are comprised of 6-bit slices 1105. These slices are designed to make the interpolators modular. FIG. 12 shows a basic 4-bit input interpolation slice.
>
> The data to the muxes comes from the subtractor (not shown). The most significant (MS) bits are either sign extension (if the slice is being used as the MS slice) or are the low order bits from the next more significant slice (when not the most significant slice). Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word. For example, for 8-bit texels, the MS slice would handle the sign bit (and no fraction bits) and the least significant (IS) slice would

> handle the fraction bits (but no sign). The slice configuration muxes separately enable or disable the slices MS portion (sign extension) or LS portion (fraction). FIG. 13 shows an 8-bit input interpolator, which is formed by coupling together two 4-bit slices. FIG. 14 shows a basic 6-bit input interpolator slice.

As is clear, at no point in this passage does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value from a data cache, as no data cache is shown or described here. One cache described by Hannah is read cache 208, shown in Figure 2, which contains mip maps used by interpolator 209. Interpolator 209 resamples the texture image to produce the output samples, which are sent to the graphics rasterizer. These mip maps are not data values used by the pending instructions in an instruction execution pipeline, to transferred into a target register, as required by the claims. Nor do the TRAM caches meet the limitations of the claims, nor the I/O caches (*e.g.* 407).

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring a first data value directly to a target register, as no registers are shown or described here. Hanna does not include any bypass circuitry that transfers any data values from a data cache to a register.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is capable of transferring the first data value without processing the first data value in a shifter circuit.

As is clear, at no point in this passage, or anywhere else in Hannah, does Hannah teach or suggest bypass circuitry, as claimed, that is associated with a load store unit.

The Examiner does not even attempt to show where these limitations may be found within Hannah or these figures, and fails to allege even a single specific element that could meet the claim limitations. Indeed, this passage of Hannah appears to be cited simply because it includes the term "bypassed". The particular sentence of Hannah the Examiner reiterates in response is "Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word." The Examiner then acknowledges that Hannah doesn't actually teach any bypass circuitry, stating:

> Hannah also teaches in column 9, lines 37-44 that his implementation of the multiplexers he minimizes gate count, e.g. reduce the size of the device, and attains "flexibility in data width." Hannah then proceeds to state that "In some applications greater precision and resolution are desirable, whereas, in other applications, speed and cost are of greater importance." This suggests that how the multiplexers are used, e.g. to bypass certain capabilities, dependent on the designers desire. Bypassing effectively disables a functionality, such as the sign extension mentioned in both Greenley and Hannah, so that it is not performed and time is not wasted on an unneeded functionality. Consequently, the speed is increased in the system.

The Examiner does not – and tacitly admits that she cannot – identify any specific circuit in Hannah that is a bypass circuitry associated with a load store unit capable of transferring a first data value from a data cache directly to a target register without processing the first data value in a shifter circuit, as claimed. To the extent anything in Hannah is bypassed at all, there is no "bypass circuitry" connected as claimed or capable of performing the claimed functions.

Since Greenley does not teach or suggest the claimed features, and Hannah does not teach or suggest the claimed features, no combination of these references can teach or suggest the claimed features. As these features are found in all independent claims, all claims distinguish over Greenley, Hannah, and any combination of them. Greenley, in fact, teaches away from the Examiner's proposed combination and further modification by teaching that the shift functions must be used for any data transfer.

Further, neither Greenly or Hannah teach or suggest doing anything in response to a determination that a pending instruction is a load word operation as recited in Claim 10. The Examiner's rejection on this point repeats both the combination above and the motivation addressed below, neither of which teach or suggest anything at all with respect to this particular limitation.

All rejections are traversed.

Applicant further notes that the Examiner's stated motivation is that "bypasses improve the performance of a system by minimizing delays from unnecessary functions (Hannah column 9, lines 38-44)". This portion of Hannah is part of the passage reproduced above, and it is clear that there is no such teaching in this passage. While Hannah teaches a trade-off between precision/resolution and speed/cost, this has nothing to do with any bypass circuitry, despite the Examiner's rhetorical bootstrapping.

Other distinctions remain, but need not be addressed at this time, as all claims are shown to distinguish over the art of record, alone or in combination.

PAGE 20/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1, 10, and 14 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-29.

PAGE 21/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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PAGE 22/22 * RCVD AT 2/28/2007 11:46:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/8 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):06-58

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